

REMARKS

The Office Action of April 1, 2002 was received and carefully reviewed. In light of the amendment presented above, reconsideration and withdrawal of the currently pending rejection is requested for the reasons advanced in detail below.

Claims 1-5 were pending prior to the instant amendment. By the above amendment, claim 1 has been amended and claims 2 and 3 canceled; consequently, claims 1, 4 and 5 remain pending in the instant application. Support for the amendments to claim 1 can be found in the specification at, for example, page 19, lines 14-17; page 20, lines 4-18; page 24, line 24 to page 25, line 8.

With respect to the rejection of claims 1-5, under 35 U.S.C. § 102(b), as being anticipated by the teachings of Jerome et al ('073), as set forth at page 2 of the Office Action, the rejection is believed to be overcome by the above amendments to claim 1. Specifically, claim 1 has been amended to more clearly define the novel features of the present invention. That is, the formation of the third insulating film is carried out such that a pair of element isolation grooves located adjacent to each other in the region other than the element formation region are continuously covered (see Figures 10, 13, element 211), during the step of forming the third insulating film, using a vapor deposition method (see specification, page 20, lines 4-18) such as employed in the deposition of the second insulating film.

The Jerome reference fails to teach the above feature of the present invention. According to Jerome, for example as shown in Figure 17, after forming the trench structure, an oxide film (element 75) is formed over the entire surface using the LOCOS method (column 8, lines 1-12) which is not a vapor deposition method. Further, the LOCOS process includes an annealing process at elevated temperatures which would inherently damage any device formed in the device region prior to the third insulating film deposition step. Therefore, the formation of the device regions, e.g., MOS

transistors, in Jerome cannot be performed after formation of the trench isolation structure (but before forming the third insulating film) since to do so would result in damage to the device caused by the LOCOS process. Finally, Jerome also teaches (Figure 8, element 50; column 6, lines 29-44) that after the filling of the trench structure a silicon oxide (third insulating film) cap can be formed by thermal oxidation, e.g., LOCOS, or vapor deposition. However, this third insulating film is formed only over the trench region and not continuously over a pair of element isolation grooves adjacent each other in an area other than the element formation region as presently claimed (and illustrated at Figures 10, 13, element 211). The vapor deposition step of Jerome (Figure 8) would require masking operations to define the trench openings to form the cap which would further complicate the process of forming isolated devices. No such masking is required by the claimed method.

In contrast to the teachings of Jerome, the presently claimed method provides the flexibility of forming the device elements before or after trench isolation structure, as well as before or after formation of the third insulating layer (see Figures 11 and 12). Further, since the pair of element isolation grooves adjacent each other in an area other than the element formation region are continuously covered by the third insulating film, the flexibility in forming the necessary wirings for the devices is increased, i.e., the third insulating film serves as insulation for the wirings.

As the Examiner is aware, MPEP Chapter 2131, requires that each and every element of the claim must be taught or be inherent in a reference in order establish anticipation of a claimed invention under 35 U.S.C. 102(b). As pointed out above, the Jerome et al ('073) reference does not teach each and every feature of the instant claims; therefore, the rejection of claims 1-5, under 35 U.S.C. § 102(b), as being anticipated by Jerome et al ('073) is believed to have been made in error and should be withdrawn.

It is believed that the present application is now in condition for allowance. However, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Lastly, it is noted that a separate Petition for Extension of Time (one month) accompanies this response along with a check in payment of the requisite extension of time fee. However, should that petition become separated from this Amendment, then this Amendment should be construed as containing such a petition. Likewise, any overage or shortage in the required payment should be applied to Deposit Account No. 19-2380 (740819-634).

Respectfully submitted,



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Marked-up Copy of Amendments

IN THE CLAIMS:

Please cancel claims 2 and 3.

Please amend claim 1 as follows: /

1. (Amended) A method for manufacturing a semiconductor device, comprising the steps of:

forming, in a semiconductor layer formed on a first insulating film, an element isolation groove extending to the first insulating film; [and]

depositing a second insulating film [in] so as to partially fill the element isolation groove by using a vapor deposition method; *claim 2*

forming an embedded layer on the second insulating film so as to completely fill the element isolation groove; and

forming a third insulating film on the embedded layer using the vapor deposition method, *claim 3*

wherein the step of forming the element isolation groove includes another step of forming an other element isolation groove adjacent to the element isolation groove in a region other than an element formation region of the semiconductor layer, and

wherein in the step of forming the third insulating film, the third insulating film is formed such that the element isolation groove and the other element isolation groove are continuously covered.